Amendments to the Specification:

Please replace the paragraph beginning at page 6, line 18 with the following amended paragraph:

In the clock input/output device configured as described above, the configuration may be~~, as recited in claim 2,~~ as follows. One of the logic gates is a two-input, one-output AND gate comprising: a first three-state inverter of which the input terminal serves as one input of the AND gate; a second three-state inverter of which the input terminal serves as the other input of the AND gate and of which the input terminal is connected to the state control terminal thereof, the second three-state inverter determining whether or not to bring the output thereof into a high-impedance state according to the state of the signal fed to the state control terminal thereof; a first inverter of which the input terminal is connected to the node between the output terminals of the first and second three-state inverters and of which the output terminal serves as the output of the AND gate; and a second inverter of which the input terminal is connected to the input terminal of the second three-state inverter and of which the output terminal is connected to the state control terminal of the first three-state inverter.

Please replace the paragraph beginning at page 7, line 13 with the following amended paragraph:

Alternatively, the configuration may be~~, as recited in claim 3,~~ as follows. One of the logic gates is a two-input, one-output OR gate comprising: a first three-state inverter of which the input terminal serves as one input of the OR gate and that receives at the state control terminal thereof the other input to the OR gate; the first three-state inverter determining whether or not to bring the output thereof into a high-impedance state according to the state of the signal fed to the state control terminal thereof; a second three-state inverter of which the input terminal serves as the other input of the OR gate; a first inverter of which the input terminal is connected to the node between the output terminals of the first and second three-state inverters and of which the output terminal serves as the output of the OR gate; and a second inverter of which the

input terminal is connected to the input terminal of the second three-state inverter and of which the output terminal is connected to the state control terminal of the second three-state ~~inverter,~~ inverter.

Please replace the paragraph beginning at page 8, line 4 with the following amended paragraph:

Alternatively, the configuration may be~~, as recited in claim 4,~~ as follows. One of the logic gates is a logic gate that selects and outputs one of two clocks according to a select signal fed thereto and that comprises: a first three-state inverter that receives at the input terminal thereof one clock and that receives at the state control terminal thereof the select signal, the first three-state inverter determining whether or not to bring the output thereof into a high-impedance state according to a signal fed to the state control terminal thereof; a second three-state inverter that receives at the input terminal thereof another clock; a first inverter of which the input terminal is connected to the node between the output terminals of the first and second three-state inverters and of which the output terminal serves as the output of the logic gate; and a second inverter that receives at the input terminal thereof the select signal and of which the output terminal is connected to the state control terminal of the second three-state inverter.

Please replace the paragraph beginning at page 8, line 18 with the following amended paragraph:

Incidentally, such a logic gate is equivalent to a circuit composed of: a first AND gate that receives the one clock; a second AND gate that receives the other clock and that also receives the select signal; an inverter that receives the select signal, inverts it, and then feeds the result to the first AND gate; and an OR gate that receives the outputs of the first and second gates. Here, the first and second AND gate may be configured ~~like the~~ as an AND gate ~~recited in claim 2,~~ comprising: a first three-state inverter of which the input terminal serves as one input of the AND gate; a second three-state inverter of which the input terminal serves as the other input of the AND gate and of which the input terminal is connected to the state control terminal

thereof, the second three-state inverter determining whether or not to bring the output thereof into a high-impedance state according to the state of the signal fed to the state control terminal thereof; a first inverter of which the input terminal is connected to the node between the output terminals of the first and second three-state inverters and of which the output terminal serves as the output of the AND gate; and a second inverter of which the input terminal is connected to the input terminal of the second three-state inverter and of which the output terminal is connected to the state control terminal of the first three-state inverter. On the other hand, ~~and~~ the OR gate may be configured ~~like the~~ as an OR gate ~~recited in claim 3~~ comprising: a first three-state inverter of which the input terminal serves as one input of the OR gate and that receives at the state control terminal thereof the other input to the OR gate; the first three-state inverter determining whether or not to bring the output thereof into a high-impedance state according to the state of the signal fed to the state control terminal thereof; a second three-state inverter of which the input terminal serves as the other input of the OR gate; a first inverter of which the input terminal is connected to the node between the output terminals of the first and second three-state inverters and of which the output terminal serves as the output of the OR gate; and a second inverter of which the input terminal is connected to the input terminal of the second three-state inverter and of which the output terminal is connected to the state control terminal of the second three-state inverter.

Please replace the paragraph beginning at page 9, line 2 with the following amended paragraph:

In the logic gate described above ~~recited in claim 4~~, according to the select signal, one of the clock fed to the first three-state inverter and the clock fed to the second three-state inverter is selected as the clock outputted from the first inverter.

Please replace the paragraph beginning at page 9, line 6 with the following amended paragraph:

In any of the clock input/output devices described above ~~recited in claims 2 to 4~~, the first inverter may be configured as a three-state inverter of which the state control terminal is grounded.

Please replace the paragraph beginning at page 9, line 9 with the following amended paragraph:

In any of the clock input/output devices configured as described above, the configuration may be~~, as recited in claim 6,~~ as follows. The three-state inverter comprises: a first transistor that receives at the first electrode thereof the supply voltage; a second transistor of which the first electrode is connected to the second electrode of the first transistor and that is of the same conductivity type as the first transistor; a third transistor of which the second electrode is connected to the second electrode of the second transistor and that is of the opposite conductivity type to the first transistor; a fourth transistor of which the second electrode is connected to the first electrode of the third transistor, of which the first electrode is grounded, and that is of the opposite conductivity type to the first transistor; and an inverter of which the output terminal is connected to the control electrode of the third transistor. Here, the node between the control electrodes of the first and fourth transistors serves as the input terminal of the three-state inverter, the node between the second electrodes of the second and third transistors serves as the output terminal of the three-state inverter, and the node between the control electrode of the second transistor and the input terminal of the inverter serves as the state control terminal of the three-state inverter.

Please replace the paragraph beginning at page 10, line 4 with the following amended paragraph:

~~As recited in claim 7, the~~ The inverter provided in the last stage of the clock input/output device may comprise: a fifth transistor that receives at the first electrode thereof the supply voltage and that is kept on during normal operation; a sixth transistor of which the first electrode is connected to the second electrode of the fifth transistor, that receives at the control electrode

thereof the clock outputted from the logic gate provided in the previous stage, and that is of the same conductivity type as the fifth transistor; a seventh transistor of which the second electrode is connected to the second electrode of the sixth transistor, that receives at the control electrode thereof the clock outputted from the logic gate provided in the previous stage, and that is of the opposite conductivity type to the fifth transistor; and an eighth transistor of which the second electrode is connected to the first electrode of the seventh transistor, of which the first electrode is grounded, that is kept on during normal operation, and that is of the opposite conductivity type to the fifth transistor. Here, the duty factor of the clock outputted from the clock input/output device is measured, in a case where one end of a resistor of which the other end is connected to the ground voltage is connected to the node between the second electrodes of the sixth and seventh transistors which serves as the output of the inverter, by measuring the current that flows through the resistor while the fifth transistor is kept on and the eighth transistor is kept off and, in a case where one end of a resistor of which the other end is connected to the supply voltage is connected to the node between the second electrodes of the sixth and seventh transistors which serves as the output of the inverter, by measuring the current that flows through the resistor while the eighth transistor is kept on and the fifth transistor is kept off.

Please replace the paragraph beginning at page 11, line 6 with the following amended paragraph:

According to another aspect of the present invention, a clock input/output device is configured~~, as recited in claim 8,~~ as follows. In a clock input/output device comprising logic gates and operating as a gate that permits a clock to pass therethrough, the inverter provided in the last stage of the clock input/output device comprises: a first transistor that receives at the first electrode thereof the supply voltage and that is kept on during normal operation; a second transistor of which the first electrode is connected to the second electrode of the first transistor, that receives at the control electrode thereof the clock outputted from the logic gate provided in the previous stage, and that is of the same conductivity type as the first transistor; a third transistor of which the second electrode is connected to the second electrode of the second

transistor, that receives at the control electrode thereof the clock outputted from the logic gate provided in the previous stage, and that is of the opposite conductivity type to the first transistor; and a fourth transistor of which the second electrode is connected to the first electrode of the third transistor, of which the first electrode is grounded, that is kept on during normal operation, and that is of the opposite conductivity type to the first transistor. Here, the duty factor of the clock outputted from the clock input/output device is measured, in a case where one end of the resistor of which the other end is connected to the ground voltage is connected to the node between the second electrodes of the second and third transistors which serves as the output of the inverter, by measuring the current that flows through the resistor while the first transistor is kept on and the fourth transistor is kept off and, in a case where one end of the resistor of which the other end is connected to the supply voltage is connected to the node between the second electrodes of the second and third transistors which serves as the output of the inverter, by measuring the current that flows through the resistor while the fourth transistor is kept on and the first transistor is kept off.